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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/320,421	05/26/99	FORBES L	303.586US1

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MM92/1108

EXAMINER	
TRAN, A	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED:
11/08/00

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trad marks

Offic Action Summary	Application No.	Applicant(s)	
	09/320,421	FORBES ET AL.	
	Examiner	Art Unit	
	Quan Tra	2816	

-- The MAILING DATE of this communication appears on the cover sheet with th correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Status

1)☒ Responsive to communication(s) filed on *25 September 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-45* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-45* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 May 1999* is/are objected to by the Examiner.

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

a)☐ All b)☐ Some * c)☐ None of the CERTIFIED copies of the priority documents have been:

1.☐ received.

2.☐ received in Application No. (Series Code / Serial Number) _____ .

3.☐ received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. & 119(e).

Attachment(s)

15) ☐ Notice of References Cited (PTO-892)
16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
17) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
18) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
19) ☐ Notice of Informal Patent Application (PTO-152)
20) ☐ Other: .

DETAILED ACTION

This office action is in response to the amendment filed 09/25/2000. A new 35 U.S.C. 112 second paragraph is introduced. The specification is also objected as being misdescriptive.

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the dual-gated transistor must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Specification

The specification is objected as being misdescriptive. Page 10, lines 16-30, describes the pair of transistors M3, M5, and M4, M6 of each inverter, B 1 and B2, comprises a dual-gated MOSFET. It is well known in the art that a dual-gated transistor is an AND function circuit. However, the pair of transistors M3, M5 and M4, M6 are the OR function circuit. Therefore, the pair of transistors M3, M5 and M4, M6 can not be replaced with a dual-gated transistor.

Claim Rejections - 35 USC ,§ 112

2. The following is a quotation of the second paragraph of 35 U. S. C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 1-45 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 1-5, 10-12, 17, 23, 25, 29, 32, 33, 37-40, 44, and 45 are misdescriptive and renders the claims indefinite as reciting the pair of transistors M3, M5 and M4, M6 is a dual-gated transistor. It is well known in the art that a dual-gated transistor is an AND function circuit. However, the pair of transistors M3, M5 and M4, M6 are the OR function circuit. Therefore, the pair of transistors M3, M5 and M4, M6 can not be replaced with a dual-gated transistor.

Claims 6-9, 13-17, 18-22, 24, 26-28, 30-31, and 41-43 are rejected as including the indefiniteness of one of the claims above.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S. C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-7, 10-14, 17-20, 29, 32-39, 44, and 45 are rejected under 35 U.S.C. 102(b) as being anticipated by Kawashima (U.S. Patent No. 5699305).

Insofar as understood to claims 1, 10, 17, 33, 35, 36, 37, Kawashima discloses in figure 7 a sense amplifier (105) comprising: a pair of cross-coupled inverters (66-69, and 72-75), wherein each inverter includes: a transistor of a first conductivity type (66, 67), a dual gated transistor of second conductivity type (68, 69, 74, 75) wherein a drain region for the dual-gated transistor is coupled to a drain region of the transistor of the first conductivity type; a pair of bit lines (IN, /IN), wherein each one of the pair of bit lines is coupled to a first gate of the dual-gated transistor in each inverter; and a pair of output transmission lines (OUT, /OUT), wherein each one of the pair of output transmission lines is coupled to the drain region of the dual-gated transistor and the drain region of the transistor of the first conductivity type in each inverter.

Insofar as understood to claims 2, 4, 11, 18, 34, and 38, figure 7 discloses the transistor of first conductivity type is a p-channel metal oxide semiconductor transistor, and the dual-gated transistor of second conductivity type is an n-channel metal oxide semiconductor transistor.

Insofar as understood to claims 29 and 32, figure 1 shows an SRAM circuit comprising a sense amplifier 29. It is inherent that the SRAM circuit is connected to a processor.

Insofar as understood to claims 3, 5, 12, 19, and 39, the drain region for the dual-gated transistor and the drain region for the PMOS transistor in one inverter is further coupled to a gate of the PMOS transistor and a second gate of the dual-gated transistor in the other inverter.

Insofar as understood to claims 6, 13, 44, and 45, the bit line capacitances are removed from the pair of output transmission lines.

Insofar as understood to claims 7 and 14, figure 1 shows that the sense amplifier circuit (29) is coupled to a number of memory cells (1-9) in an array of memory cells.

Insofar as understood to claim 20, figure 1 shows a sense amplifier circuit (29) included in a memory circuit.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U. S. C. 103 (a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 8, 9,15-22, 30, and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kawashima (U.S. Patent No. 5699305).

As to claims 8, 9, 15, 16, 21, and 22, 30, and 31, Kawashima's figure 7 shows all elements of the claimed invention except that it does not show the value of the supply voltage is less than 1.0 Volts and the output delay times is less than 10 ns. However, the selection of the supply voltage value to be less than 1.0 Volts and the output delay times to be less than 10 ns is seen as an obvious design expedient dependent upon the particular environment of use to ensure optimum performance.

8. Claims 23-28 and 40-43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kaneko et al. (U.S. Patent No. 6069828) in view of Kawashima (U.S. Patent No. 5699305).

Insofar as understood to claim 23, Kaneko et al. teaches in figure 2 a memory circuit comprising a number of memory arrays (two sides of sense amplifier 15); a sense amplifier (15), a complementary pair of bit lines (BL1, BL1, BL2, BL2) input to the sense amplifier. Thus, figure 2 shows all elements of the claim except that it does not show the sense amplifier comprising a pair of cross-coupled inverters, wherein each inverter includes a dual-gated NMOS transistor coupled in series with a p-channel transistor. However, Kawashima shows in figure 7 a sense amplifier circuit comprising a pair of cross-coupled inverters, wherein each inverter includes: a PMOS transistor (66, 67), a dual-gated NMOS transistor (68, 69, 74, 75) wherein the drain region for the dual-gated NMOS transistor is coupled to a drain region of the PMOS transistor; a pair of bit lines (in, /in), wherein each one of the pair of bit lines is coupled to a first gate of the dual-gated transistor in each inverter; and a pair of output transmission lines (out, /out), wherein each one of the pair of output transmission lines is coupled to the drain region of the dual-gated NMOS transistor and the drain region of the PMOS transistor in each inverter for the purpose of operating at a high speed. Therefore, it would have been obvious to one having an ordinary skill in the art to use the sense amplifier circuit of Kawashima into the sense amplifier (15) of Kaneko et al.'s figure 2 for operate at high speed.

As to claim 24, Kawashima's figure 1 shows a folded bit line memory circuit.

As to claims 25, the drain region for dual-gated NMOS transistor and the drain region for the PMOS transistor in one inverter is further coupled to the gates of the PMOS transistor and a second gate of the dual-gated NMOS transistor in the other inverter.

As to claims 28 and 40, Kaneko et al.'s figure 2 shows number of equilibration (14a, b) and a number of isolation (18a, b) transistors coupled to the complementary pair of bit lines.

As to claims 26, 27, 41, and 42, the selection of the supply voltage value to be less than 1.0 Volts and the output delay times to be less than 10 ns is seen as an obvious design expedient dependent upon the particular environment of use to ensure optimum performance.

As to claim 43, Kawashima's figure 7 shows a step of removing the bit line capacitance from the output nodes.

Response to Arguments

9. Applicant's arguments filed 09/25/2000 have been fully considered but they are not persuasive. The "dual-gated transistor" in the claims is misdescriptive, see the reason above. Therefore, the previous rejection is maintained.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. These references are cited as interest because they show some circuits analogous to the claimed invention.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quan Tra whose telephone number is (703) 308-6174. The examiner can normally be reached on Monday to Friday from 7:40 am to 4:20 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reach at (703) 308-4876. The fax phone number for this group is (703) 308-7722.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956.

QT

Terry D. Cunningham
Primary Examiner

October 24, 2000